We Claim:

1. A trench transistor, comprising:

a semiconductor body of a first conduction type having a surface region;

a semiconductor region of a second conduction type opposing said first conduction type provided in said surface region of said semiconductor body and having an uncovered surface defining a top;

said semiconductor body and said semiconductor region having a trench formed therein and extending from said top downward from said uncovered surface of said semiconductor region through said semiconductor region as far as said semiconductor body, said trench having a wall, a lower region, and an upper region;

an insulation layer at least partially lining said wall of said trench and having an upper end;

a conductive trench filling disposed in said lower region of said trench and having a top side;

an insulating trench filling disposed in said upper region of said trench, having a surface, and adjoining said top side of said conductive trench filling; and

a semiconductor zone of said first conduction type provided along said insulation layer in said semiconductor region and having a lower edge;

said upper end of said insulation layer and said surface of said insulating trench filling at least partially projecting above said surface of said semiconductor region;

said lower edge of said semiconductor zone lying lower than said top side of said conductive trench filling;

a spacer provided along said insulation layer and projecting above said surface of said semiconductor region and serving as a dopant source for said semiconductor zone; and

a channel zone running along said insulation layer in said semiconductor region.

2. The trench transistor according to claim 1, wherein said surface of said semiconductor region has a trench formed between two cells.

3. The trench transistor according to claim 1, further comprising a silicide layer making contact between said semiconductor region and said semiconductor zone.

4. The trench transistor according to claim 1, wherein said semiconductor region has a contact zone.

5. The trench transistor according to claim 4, wherein said contact zone is implanted.

6. The trench transistor according to claim 1, further comprising an insulating spacer layer underlying said spacer.

7. The trench transistor according to claim 1, wherein said spacer is made of a material selected from the group consisting of polycrystalline silicon, a metal provided with dopant, borophosphosilicate glass, phosphosilicate glass, and borosilicate glass.

8. The trench transistor according to claim 6, wherein said insulating spacer layer is made of a material selected from the group consisting of silicon nitride and silicon oxide.

9. The trench transistor according to claim 1, wherein said semiconductor body is made from a material selected from the

group consisting of silicon, silicon carbide, and a compound semiconductor.

10. The trench transistor according to claim 1, further comprising further electrodes disposed in said trench.

11. The trench transistor according to claim 1, further comprising a field plate disposed in said trench.

12. A trench transistor, comprising:

a semiconductor body of a first conduction type having a surface region;

a semiconductor region of a second conduction type opposing said first conduction type, provided in said surface region of said semiconductor body, having an uncovered surface defining a top and a trench formed therein; said trench having an upper region, a lower region, and a wall, and extending from said top downward from said uncovered surface of said semiconductor region through said semiconductor region as far as said semiconductor body;

an insulation layer at least partially lining said wall of said trench and having an upper end;

an insulating trench filling disposed in said upper region of said trench and having a surface;

a conductive trench filling disposed in said lower region of said trench having a top edge adjoining said insulating trench filling;

a semiconductor zone of said first conduction type provided along said insulation layer in said semiconductor region and having a lower edge;

said upper end of said insulation layer and said surface of said insulating trench filling at least partially projecting above said surface of said semiconductor region; and

said lower edge of said semiconductor zone lying lower than said top side of said conductive trench filling; and

a body contact zone of said second conduction type provided between two semiconductor zones having a doping of said first conduction type of two adjacent cells and produced by reversing the doping of regions of the two semiconductor zones.

13. The trench transistor according to claim 12, wherein said semiconductor body is made from a semiconductor material

selected from the group consisting of silicon, silicon carbide, and a compound semiconductor.

14. The trench transistor according to claim 12, further comprising electrodes disposed in said trench.

15. The trench transistor according to claim 12, further comprising a field plate disposed in said trench.

16. A method for fabricating a trench transistor, which comprises:

providing a semiconductor body of a first conduction type having a surface region;

providing a semiconductor region of a second conduction type opposing the first conduction type in the surface region of the semiconductor body and having an uncovered surface defining a top;

etching a trench in the semiconductor body and the semiconductor region extending from the top downward from the uncovered surface of the semiconductor region through the semiconductor region as far as the semiconductor body, the trench having a wall, a lower region, and an upper region;

at least partially applying an insulation layer to the wall of the trench, the insulation layer having an upper end;

disposing a conductive trench filling in the lower region of the trench, the conductive trench filling having a top side;

disposing an insulating trench filling with a surface in the upper region of the trench on the top side of the conductive trench filing;

removing the semiconductor body between two trenches of adjacent cells to expose a sidewall of the insulation layer projecting above the now-removed surface of the semiconductor layer;

subsequently applying a spacer made from conductive material along the sidewall of the insulation layer; and

introducing dopant from the spacer into the semiconductor body to form a semiconductor zone of the first conduction type in the semiconductor region.

17. The method according to claim 16, which further comprises forming a semiconductor region of the second conduction type before the semiconductor zone has been produced.

18. The method according to claim 16, which further comprises forming a semiconductor region of the second conduction type after the semiconductor zone has been produced.

19. The method according to claim 16, which further comprises, after the forming of the semiconductor zone of the given conduction type, applying a further spacer layer over the spacer by introducing a trench and removing the further spacer layer.

20. The method according to claim 16, which further comprises, after the forming of the semiconductor zone of the given conduction type, applying a further spacer layer over the spacer by introducing a trench and etching back the further spacer layer.

21. A method for fabricating a trench transistor, which comprises:

providing a semiconductor body of a first conduction type having a surface region;

providing a semiconductor region of a second conduction type opposing the first conduction type in the surface region of the semiconductor body, the semiconductor region having an uncovered surface defining a top;

etching, in the semiconductor region, a trench having a an upper region, a lower region, and a wall, and extending from the top downward from the uncovered surface of the semiconductor region through the semiconductor regions as far as the semiconductor body;

applying an insulation layer with an upper end to at least partially line the wall of the trench;

forming an insulating trench filling with a surface in the upper region of the trench;

forming a conductive trench filling with a top edge in the lower region, the conductive trench filling adjoining the insulating trench filling;

removing a semiconductor body between two trenches of adjacent cells;

forming a semiconductor region of a second conduction type;

subsequently introducing a semiconductor zone of the first conduction type substantially over an entire surface between the trenches;

then applying an insulating spacer layer to the semiconductor zone in a region of the insulation layer;

then implanting a body contact zone between the spacer layers of adjacent cells; and

finally at least partially removing the spacer layer.

22. The method according to claim 21, wherein the semiconductor zone is introduced by low-dose implantation.

23. The method according to claim 21, which further comprises completely removing the insulating spacer layer.